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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/855,899	05/15/2001	Hendrik Rotsch	A34306	1159
7590	09/03/2004		EXAMINER	
Andreas Grubert Baker Botts L.L.P. 910 Louisiana Street One Shell Plaza Houston, TX 77002-4995			GOSHTASBI, JAMSHID	
			ART UNIT	PAPER NUMBER
			2637	
DATE MAILED: 09/03/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/855,899	ROTSCH ET AL.
	Examiner Jamshid Goshtasbi-G.	Art Unit 2637

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) Responsive to communication(s) filed on 05/15/2001.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) Claim(s) 1-9 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1,2 and 4-8 is/are rejected.  
 7) Claim(s) 3 and 9 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 15 May 2001 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date #8.	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

**DETAILED ACTION**

1. Claims 1-9 are pending in the application.

***Drawings***

2. The drawings are objected to because the rectangular boxes in figures 1-3 are should be provided descriptive text labels. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. In addition to Replacement Sheets containing the corrected drawing figure(s), applicant is required to submit a marked-up copy of each Replacement

Sheet including annotations indicating the changes made to the previous version.

The marked-up copy must be clearly labeled as "Annotated Marked-up Drawings" and must be presented in the amendment or remarks section that explains the change(s) to the drawings. See 37 CFR 1.121(d). Failure to timely submit the proposed drawing and marked-up copy will result in the abandonment of the application.

### ***Claim Objections***

4. Claim 6 and is objected to under 37 CFR 1.75(c), as being of improper dependent form. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

**Claim 6** does not refer to a preceding claim; instead, it is improperly dependent on Claim 9.

### ***Claim Rejections - 35 USC § 112***

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

**Claim 6** is dependent on Claim 9, where Claim 9, itself, is dependent on Claim 6, creating a dependency loop that renders Claim 6 indefinite.

***Claim Rejections – 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1, 2, 5, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanai et al. (US 5003559) in view of Southard (US 4598257).

As to **Claim 1**, Kanai et al. discloses a digital transmission system (method) with the transmission unit transmitting synchronization signals (see figures 3 and 5A-57; col. 2, lines 4-15; col. 3, lines 4-15) to a reception unit; the receiver extracting the received synchronization signals; and supplying it to a clock generator [transmitter] that outputs a stable number of jitter-free (col. 3, line 30) clock signals, with predetermined frequency, and phase-locked with [and between two] synchronizing signals (col. 2, lines 16-36; col. 3 lines 16-20; col. 5, line 21 to col. 6, line 3) [because, the fact that each clock generation starts with detection of a synch signal, means that the receiver clock generates a stable (constant) number of clock signals between two synch signals]; Kanai et al., however, fails to teach the use of a second clock generator [transmitter] that is driven by the first generated clock signal and that is continuously present even when the first clock signals are absent; neither does Kanai et al. teaches how and whether the second clock signal is phase synchronized with the first

clock signal; however, Southard teaches that since the signal transmitted from the master clock [in a transmitter] to a slave clock [in a receiver] is subject to wander (frequency variation) and jitter (phase variation) and may lose its integrity or disappear completely (col. 1, lines 62-65), the slave clock [in the receiver] must be equipped to discern the average frequency of the master [in the transmitter] clock signal and to take quick remedial action upon detection of failure (col. 1, line 68 to col. 2, line 5), and must be capable of being maintained on a routine basis, or repaired if a failure occurs, while maintaining a stable and synchronized [with the received reference clock] signal output; Southard, also, teaches that it is known to use a receiver (slave) clock comprising of at least two redundant [clock signal generating] units, operating in synchronization with each other and with the transmitted reference clock, so that one [clock signal generating] unit can be removed and maintained or repaired while the other unit continues to operate and, ideally, being possible to switch from one of the two redundant clock units to the other while maintaining a constant frequency (slip free) and constant phase (glitch free) output signal (col. 2, lines 6-18); further, Southard discloses an apparatus that includes a first and a second clock generator (CCG) that operate in master and slave relationship, each clock generator unit comprising a controllable oscillator for generating and presenting a clock pulse signal and a device for controlling the oscillator so as to maintain the frequency of the clock pulse signal substantially constant (in the case where the subject clock generator is operating as a "master") or to cause the frequency and phase of this clock pulse signal to closely follow the frequency and phase of

the clock pulse signal produced by the other clock generator (in the case where the subject clock generator is operating as a "slave") (col. 3, lines 26-39); further, the master CCG is operative either to produce a stable clock signal of its own or to follow the external reference clock signal, and the slave CCG operates to produce [using the stable clock signal being supplied to it by the first clock generator] an output clock signal which is identical in frequency and substantially identical in phase to the frequency and phase, respectively, of the output clock pulse signal produced by the master CCG (col. 3, lines 55-62); further, should the master CCG become faulty [absent], it is possible to reverse the master slave relationship without the slightest phase slip or discontinuity in the output signal (col 3, lines 66 to col. 4, line 7); further, each CCG contains a microprocessor based intelligent phase lock loop (PLL) (col. 6, lines 47-49) and the slave CCG closely follows the frequency and phase of its master partner by executing its very accurate frequency and phase locking algorithm (col. 14, lines 22-27) and adjusts for the phase difference between its clock signal and the master CCG clock signal by changing the frequency of the slave CCG clock signal (col. 16, lines 23-26). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Southard into the method of Kanai et al. for producing the claimed invention because incorporating the redundant CCG clock signal generating method of Southard in Kanai et al. digital transmission method provides for a continuous and stable clock signal in the receiver unit that is synchronized with an extracted reference clock signal of the transmitter (an external reference

clock) wherever an uninterrupted (and in synchronization with a transmitted synchronization instruction) data processing is needed.

**Claim 2** inherits the limitations of Claim 1; further, Southard teaches that the fine phase measurements are used as input to a proportional control path and an integral control path that are added together with the frequency offset function (coarse integral part) and the modulation function to control the voltage controlled crystal oscillator (col. 10, lines 35-42); and that the execution of a routine in the slave CCG changes the frequency of the slave CCG clock signal slightly so that the phase of this clock signal will drift with respect to the phase of the master CCG clock signal; and that this phase drift is allowed to continue for 1 second; the entire fine phase locking procedure should not exceed a prescribed maximum time period (col. 19, lines 51-54). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Southard into the method of Kanai et al. for producing the claimed invention because incorporating the slight phase drift of the second (slave) CCG allows for fine (soft) synchronization.

**Claim 5** inherits the limitations of Claim 1; further, Southard teaches that the first clock generator includes a control means that includes a digital phase comparator means for comparing the phase of the first clock pulse signal with the phase of a reference clock signal [the received clock signal; synchronization signals] and producing a first digital signal representative of the difference in phase; and a processing means comprising a digital microprocessor, connected to said first phase comparator means, for producing said first control signal in

response to said first digital signal (col. 23, lines 55-64). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Southard into the method of Kanai et al. for producing the claimed invention because incorporating the supplying the synchronization signal (extracted transmitted clock signal) via a phase regulator (phase comparator and frequency controller) of a PLL provides means for generating a stable clock signal in synchronization with the received reference clock signal.

As to **Claim 7**, the claimed reception unit for synchronizing signals recites features that correspond with subject matter mentioned above in the rejection of Claim 1 and are applicable hereto.

**Claim 8** inherits the limitations of Claims 5 and 1; further, Kanai et al. discloses the receiver clock that generates clock signals of a predetermined frequency (nominal number of clock signals) in phase-locked relationship with synchronizing signal (col. 3, lines 17-21; col. 5, lines 22-27); further, Kanai et al. teaches a synchronizing signal 2FSR is supplied to a phase comparator circuit of the PLL circuit, wherein it is phase-compared with a fed-back signal [a basic clock signal, having frequency close to the reference clock signal] from a frequency divider, where, a phase comparison error signal is then converted to a direct current voltage by a loop filter, and the oscillating frequency of an oscillator (not shown) is controlled on the basis of this direct current voltage; further, Southard teaches that a microprocessor controlled digital phase lock loop operates to control each of the two clock signal generators such that the

instantaneous dynamic phase difference does not exceed the phase noise of the voltage controlled crystal oscillators of the phase lock (Abstract). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Southard into the method of Kanai et al. for producing the claimed invention because incorporating the phase regulation method of Southard into the first clock of Kanai et al. provides for generation of a clock signal of a predetermined stable frequency that is fine synchronized with the received synchronization signal.

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kanai et al. (US 5003559) in view of Southard (US 4598257) as applied to claim 2 above, and further in view of Gegner et al. (US 4565975).

Claim 4 inherits the limitations of Claim 1 or 2; further, Gegner et al. discloses that a clock signal T2 is generated that is synchronous with the original sending pulse (in interference free operations), and is used for synchronously detection of the incoming digital signals (col. 5, lines 3-9); further, in the case of longer lasting interference [absence of the first clock pulse, or the synch signal], the oscillator VCO (using a reference voltage) generates the clock pulse T3 at a predetermined (nominal) frequency (col. 3, lines 37-42; col. 4, lines 27-29; col. 8, lines 37-41); Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Gegner et al. into the method of Kanai et al. (in view of Southard) for producing the claimed invention because controlling the oscillator of the second clock with a reference

voltage, in the absence of the first clock signal, drives the second clock generator with a prescribed nominal frequency.

***Allowable Subject Matter***

10. Claims 3, and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusions***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ott [US 6154508], Ohdachi [US 6230021 B1], and Stessen et al. [US 6297849 B1] all teach various aspects of using of PLL and frequency dividers and the generation of more than one clock signals in a methods and systems for synchronization of communicating digital systems.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jamshid Goshtasbi-G. whose telephone number is (571) 272-3012. The examiner can normally be reached on M-F 8:00/4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jamshid Goshtasbi-G.  
Examiner  
Art Unit 2637

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PRIMARY EXAMINER  
9/2/04